

# MEASURE MULTIPLE ANALOG INPUTS USING ANALOG MUX BUS

|                                  |                              |
|----------------------------------|------------------------------|
| <b>Project Name:</b>             | Example_Analog_Mux_Bus_24x94 |
| <b>Associated Part Families:</b> | CY8C24x94, CY7C64215         |
| <b>Software Version:</b>         | PSD5.0 SP5                   |
| <b>Programming Language:</b>     | C                            |
| <b>Related Hardware:</b>         | CY3214                       |
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## PROJECT OBJECTIVE

Demonstrate the usage of Analog Mux bus to measure analog signals from any pin (except Port 7 pins).

## OVERVIEW

The project measures 0-5V signals present on P0[3], P0[5], P3[1] and P3[6] and displays the 14 bit signed ADC value on an LCD. The project uses the MUX\_CRx registers to connect and disconnect the signals to the Analog Mux bus which is connected to a unity gain PGA and a 14 bit incremental ADC. The project can be tested on the CY3214 Evaluation board from Cypress Semiconductors.

## USER MODULE LIST AND PLACEMENT

The following table lists user modules used in this project and the hardware resources occupied by each user module.

| User Module | Placement    |
|-------------|--------------|
| ADCINC      | ASC10, DBB00 |
| PGA         | ACB00        |
| LCD         | Port4        |

## GLOBAL RESOURCES

| Important Global Resources |                  |   |
|----------------------------|------------------|---|
| Parameter                  | Value            | Comments                                  |
| CPU_Clk                    | SysClk/2         | Set CPU Clock to 12MHz                    |
| VC1                        | 6                | This sets the column clock to ADC as 4MHz |
| Analog Power               | SC On / Ref High | See Note below                            |
| RefMux                     | Vdd/2 +/- Vdd/2  | Range of ADC set to 0V to Vdd             |

### Note:

The Reference power has to be set to the maximum power level used by the resources in the project. For example, if there is an ADC operating at Medium power and a PGA operating at High Power, the Reference power should be set to High. Similarly, if there is a PGA operating at Medium power and a Filter operating at Low Power, the Reference power should be set to Medium.

## USER MODULE PARAMETER SETTINGS

The following tables show the user module parameter settings for each of the user modules used in the project.

| PGA       |                            |  |
|-----------|----------------------------|--|
| Parameter | Value                      | Comments                               |
| Gain      | 1.000                      |  |
| Input     | AnalogColumnMuxBusSwitch_0 | Input comes through the mux bus switch |
| Reference | AGND                       |  |

|           |         |  |
|-----------|---------|--|
| AnalogBus | Disable |  |
|-----------|---------|--|

## Notes:

The Analog\_MuxBus\_0 is connected to the input to the PGA through the AnalogColumnMuxBusSwitch\_0.

| ADCINC       |              |   |
|--------------|--------------|---|
| Parameter    | Value        | Comments                                      |
| DataFormat   | Signed       | For single ended input this would be unsigned |
| Resolution   | 14 bits      |   |
| Data Clock   | VC1          | Clock to ADC is VC1 = 4MHz. See note below    |
| ClockPhase   | Norm         | See Note below                                |
| PosInput     | ACB00        | The input to ADC is from the PGA              |
| NegInput     |              | Not used                                      |
| NegInputGain | Disconnected |   |
| Pulsewidth   | 1            | Left at default value. Not used               |
| PWM Output   | None         | PWM output is not used                        |

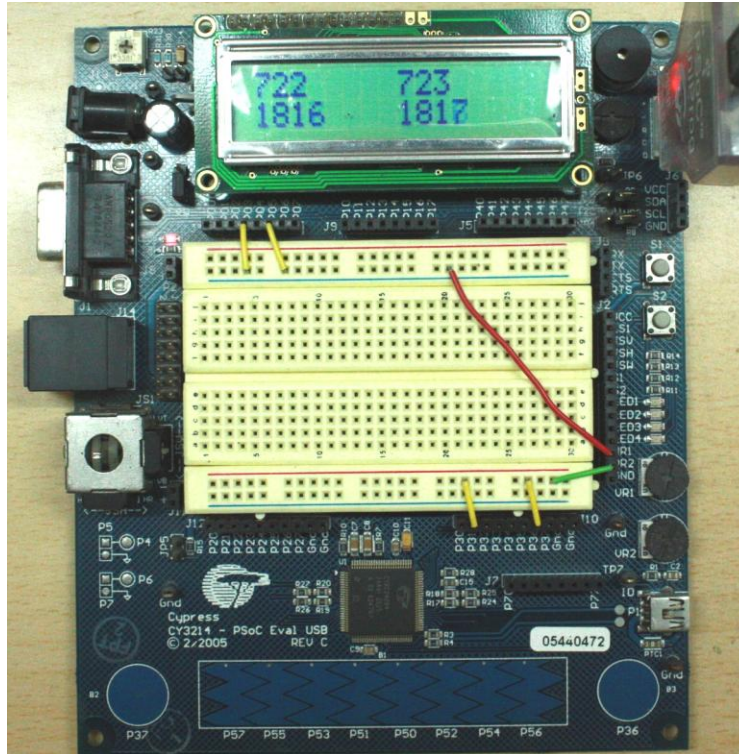
## Notes:

- The Data Clock parameter of the ADC selects the clock that is fed to the digital section of the ADC. For the correct operation of the ADC, the Column clock of the ADC should be set to the same clock source.
- When the input to the ADC is from an adjacent switched capacitor block, then the clock phase should be set to Swapped. For continuous signals like from a CT block, direct port pin or from the analog bus, the clock phase can be either Norm or Swapped.

| LCD       |         |  |
|-----------|---------|--|
| Parameter | Value   | Comments   |
| LCD_Port  | Port_4  | Port_4 is used for LCD as this is the port used for LCD connection in the CY3214 board |
| Bargraph  | Disable | Bargraph function not used   |

**HARDWARE**

The project can be tested on the CY3214 evaluation board from cypress. The analog signals are taken from VR1 and VR2, two potentiometers. Each potentiometer is connected to two analog input pins. VR1 is connected to P0[3], P0[5] and VR2 is connected to P3[1] and P3[6]. The photograph of the test setup is shown below.



## OPERATION

On power up, the code in boot.asm is executed. The device configuration is loaded inside boot.asm and all the hardware resources are configured as they are defined in the device editor. After the hardware resources are configured, main.c is executed. The following operations are performed inside main.c.

- Global interrupts are enabled. Though this project does not use any interrupts, the ADC requires the interrupts to be serviced. So, enabling global interrupts is necessary.
- The PGA and the ADC are started at High Power.
- The LCD is initialized.
- The SplitMux bit is cleared in the DAC\_CR register. This connects the left and right side Analog Mux buses thus making a single mux bus.
- Inside an infinite loop, the following operations are performed
  - The function ReadADCChannel is called with channel numbers 0, 1, 2, 3.
  - This function connects the corresponding port pin to the analog mux bus using the MUX\_CRx register and performs a single sample on the ADC and returns the result. A small delay is introduced after connecting the signal to the analog mux bus to allow the op-amp to settle. The delay depends on the power level of the PGA. For high power, the delay can be less than 1uS. For low power, the delay should be 6uS. Refer AC Op amp specification in the device data sheet.
  - After acquiring all the 4 input signals, the results are displayed as ASCII on the LCD. The conversion to ASCII is done by calling the itoa function.

## REFERENCES

- PSoC Technical Reference Manual, Section 20.1.2 Two Column Analog Input Configuration, Figure 20-4.

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