Measure and Display 0-5V on an LCD

Project Name: Example_Measure_5V
Programming Language: C
Associated Part Families: CY8C29/27/24/22xxx,CY8C23x33, CY8CLED04/08/16, CY8CNP102, CY8C28x45
Software Version: PD 5.0

Project Objective

This project is designed to measure a 0 to 5V input using ADCINCVR and display it on an LCD

Overview

A 0 to 5V input voltage applied to P0[1] is measured using an ADCINCVR configured with 12 bit resolution. The ADC value is converted into a floating point value that represents the input voltage and then is displayed on the LCD.

User Module List and Placement

The following table lists user modules used in this project and the hardware resources occupied by each user module.

User Module	Placement
PGA	ACB00
ADC (ADCINCVR)	ASC10
LCD	Port_2

User Module Parameter Settings

The following tables show the user module parameter settings for each of the user modules used in the project.

PGA		
Parameter	**Value**	**Comments**
Gain	1.00	The PGA is set as a unity gain buffer
Input	AnalogColumn_InputMUX_0	Input comes from P0[1] via AnalogColumn_InputMUX_0
Reference	VSS	Reference to PGA is set to VSS
AnalogBus	Disable	As the output of the PGA is used internally, the analog bus is disabled

Notes:

- PGA is used as a buffer is this application
- When measuring uni-polar signals referenced to VSS, the reference for the PGA should be set to VSS. When measuring bipolar signals around AGND, the Reference should be set to AGND.

LCD		
Parameter	**Value**	**Comments**
LCD Port	Port_2	Port 2 is used for LCD
BarGraph	Disable	Bar Graph is not used in this project so it is disabled

ADC		
Parameter	**Value**	**Comments**
Input	ACB00	Input to ADC comes from the PGA in ACB00
Clock Phase	Norm	See Note below
Clock	VC1	This is the clock to the ADC. The sample rate of the ADC is decided by the clock. Make sure that the column clock to the ADC is the same as this setting
ADCResolution	12	ADC is configured for 12 bit resolution
CalcTime	10	See note below
DataFormat	Unsigned	Get unsigned value from ADC to keep single ended input 0-5V

Notes:

- As the Clock to the ADC is set to VC1, the column clock for Analog Column 0 should be set to VC1.
- When the input to the ADC comes from another SC Block, the clock phase should be set to Swapped. This is because the output of the SC block is valid during Phase-2 and is zero during Phase-1. If the ADC clock is set to Norm, the ADC will sample the output of the SC block during Phase-1 and will always read Zero. If the input to the ADC comes from a continuous signal source like CT block, Analog Bus or a direct port pin, the ClockPhase may be set to “Norm” or “Swapped”
- The CalcTime is the number of data clocks the ADC holds the result after conversion. The CPU has to read the result within this duration. The minimum value for CalcTime is calculated from the data clock, CPU clock and the number of CPU clocks required to read the result inside the ADC’s ISR. If your application has other interrupts running, there is a chance that the CPU is busy in other ISRs when the ADC has completed the conversion. In this case, add the worst case CPU clocks that may be consumed by other ISRs in the calculation of CalcTime parameter. This will ensure that the ADC result is not corrupted by the next conversion in case the CPU cannot read the ADC result at the end of conversion. Refer the User module data sheet for the formula to calculate calc time.

Global Resources

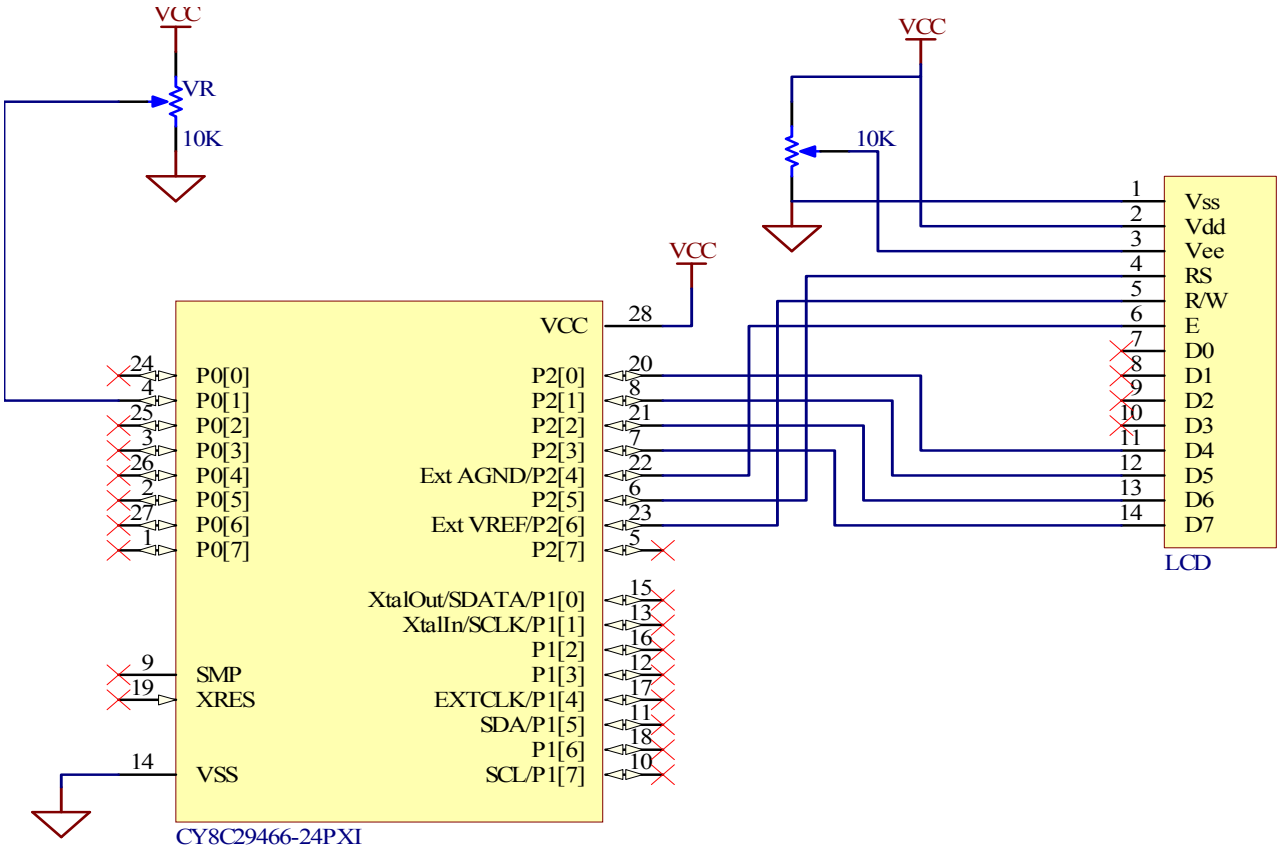
Important Global Resources		
Parameter	**Value**	**Comments**
Power Setting	5.0V/ 24MHz	Circuit is supposed to operate at 5V Vdd and IMO is supposed to generate 24MHz
CPU Clock	SysClk/2	CPU will run at 12MHz
VC1=SysClk/N	6	24/6 = 4Mhz. This clock is used as the column clock for SC blocks and clock to TMR and CNT blocks of ADC.
SysClk Source	Internal24_MHz	Clock source is kept as IMO
Analog power	SC On/Ref High	SC blocks are kept on and power is set to High
Ref Mux	(Vdd/2) +/- (Vdd/2)	The analog reference is set to measure from VSS to VDD

Notes:

- The Analog Power should be set to SC On / Ref High. If the power is set to SC Off, all SC blocks are disabled and hence the ADC will not work.
- The Global Resources relevant to this project operation are shown above. Other global resources may be left at their default value or configured as required.

Hardware Connections

The schematic diagram for the project is shown below.



The LCD is connected to Port2 of the PSoC. The analog input is connected to P0[1]. The project may be tested using the CY3210 PSoCEval1 board.

- Connect LCD to J9 on the CY3210 board
- Connect VR pin of J5 to P0[1] on J6

Operation

On reset, device configuration is loaded and then code in main.c is executed.

Following are the operations performed by firmware:

- PGA is started in HIGHPOWER mode.
- LCD is started.
- On LCD at location 0,0 “MEASURED VOLTAGE” is printed.
- Then global interrupts are enabled.
- ADC is started in HIGHPOWER mode and the conversion is started in continuous sampling mode.
- The scale factor to convert the ADC counts to voltage is calculated and stored in variable fScaleFactor. The scale factor is calculated as Volts / Count. The input voltage range is 5V and the number of ADC counts is 4096. So, the scale factor is 5V / 4096
- In an infinite loop following operations are performed:
  - Wait until ADC data is available.
  - Read ADC Data into variable iData and clear ADC flag.
  - Multiply the ADC result by fScaleFactor to get the value of input voltage. In the multiplication, the variable iData is typecast into a float.

- Convert this float value in ASCII string using function ftoa. The function returns a pointer to the string that holds the converted ASCII value. To use this function stdlib.h header file is included in project.
- Display this ASCII string on LCD at location row 1 column 0 followed by string “V”.

To test the project, vary the input voltage on P0[1] and observe the value displayed on the LCD.

Note: When varying the input voltage from 0 to 5V, it will be observed that the display will not vary exactly from 0V to 5V. Instead the display will vary from a few tens of millivolts above zero to a few tens of millivolts below 5V. This is because the output of the PGA is not rail to rail, and is in the range of about (VSS+50mV) to (VDD-50mV). This is an expected behavior.

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